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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/699,321 | 10/31/2003 | Stewart Logie | 10069/26 | 2545 |

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| EXAMINER | |
|---|---|
| FENTY, JESSE A | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2815 | |

DATE MAILED: 05/24/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Supplemental

# Office Action Summary

| Application No. | Applicant(s) | |
|---|---|---|
| 10/699,321 | LOGIE, STEWART | |
| **Examiner** | **Art Unit** | |
| Jesse A. Fenty | 2815 | |

*-- Th MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *31 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5-10 and 12-20* is/are rejected.

7)☒ Claim(s) *4 and 11* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *01/29/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Claim Rejections - 35 USC § 102*

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1, 3 and 7 are rejected under 35 U.S.C. 102(e) as being anticipated by Yu (US 2003/0213971 A1).

In re claim 1, Yu (Figs. 7C, 7F) discloses a semiconductor device, comprising:

A substrate (112) having a first junction region (116) separated from a second junction region (118) by a substrate region;

A MOS gate electrode (148) overlying the substrate region and separated therefrom by a gate oxide layer (146);

Dielectric sidewall spacers adjacent to opposing sides of the MOS gate electrode and overlying the substrate region;

Wherein the substrate region is defined by a uniformly doped region (N-well 112) of the substrate between the first junction region and second junction region.

In re claim 3, Yu discloses the device of claim 1, wherein the first junction region (116) comprises a semiconductor material of the first conductivity type, and the second junction region (118) comprises a semiconductor material of a second conductivity type.

In re claim 7, Yu discloses the device of claim 1, wherein the gate electrode is electrically coupled to the substrate.

3. Claims 1, 2 and 7 are rejected under 35 U.S.C. 102(e) as being anticipated by Hu et al. (US 2003/0201498 A1).

In re claim 1, Hu (Fig. 3A) discloses a semiconductor device, comprising:

A substrate (10) having a first junction region (22) separated from a second junction region (22) by a substrate region;

A MOS gate electrode (42) overlying the substrate region and separated therefrom by a gate oxide layer (146);

Dielectric sidewall spacers (41) adjacent to opposing sides of the MOS gate electrode and overlying the substrate region;

Wherein the substrate region is defined by a uniformly doped region (10) of the substrate between the first junction region and second junction region.

In re claim 2, Hu discloses the device of claim 1, wherein first and second junction regions comprise a semiconductor material of the same conductivity type.

In re claim 7, Hu discloses the device of claim 1, wherein the gate electrode is electrically coupled to the substrate.

4. Claims 1, 2, 6, 8-10 and 12-20 are rejected under 35 U.S.C. 102(e) as being anticipated by Lin et al. (US 2003/0173630 A1).

In re claim 1, Lin (Fig. 3) discloses a semiconductor device, comprising:

A substrate (30) having a first junction region (14a) separated from a second junction region (14b) by a substrate region;

A MOS gate electrode (12) overlying the substrate region and separated therefrom by a gate oxide layer;

Dielectric sidewall spacers adjacent to opposing sides of the MOS gate electrode and overlying the substrate region;

Wherein the substrate region is defined by a uniformly doped region (P-substrate) of the substrate between the first junction region and second junction region.

In re claim 2, Lin discloses the device of claim 1, wherein first and second junction regions comprise a semiconductor material of the same conductivity type (N+).

In re claim 6, Lin discloses the device of claim 1, wherein the device is configured to support a voltage of greater than about 2.5 volts is across the first and second junction regions (section [0040], Table 1).

In re claim 8, Lin discloses the device of claim 1, wherein at thickness of the gate oxide layer is substantially the same as a gate oxide thickness of the MOS circuit (section [0019], low-voltage transistors will have the same gate oxide thickness).

In re claim 9, Lin (Fig. 3) discloses a semiconductor device, comprising:

A voltage supply node (Pad) and a ground node (Vss);

An MOS circuit coupled to the voltage supply node and the ground node;

A transistor having a first junction region (14b) coupled to the voltage supply node, a second junction (14a) coupled to the ground node, and a substrate region between the first and second junction regions;

An MOS gate electrode (12) overlying the substrate region and separated therefrom by a gate oxide layer; and

Dielectric sidewall spacers adjacent to opposing sides of the MOS gate electrode and overlying the substrate region,

Wherein the substrate region comprises a junction-free semiconductor region (no LDD regions) between the first and second junction regions.

In re claim 10, Lin discloses the device of claim 9, wherein the transistor functions as a junction diode (section [0051]) such that the first junction region comprises a cathode and the second junction region comprises an anode.

In re claim 12, Lin discloses the device of claim 10, wherein the transistor comprises a plurality of 1 to N forward biased diodes connected in series (represented by the multiple gate regions with thin gate oxide layers and corresponding P/N junctions), such that the first junction region of the first diode is coupled to the voltage supply node and the second junction region of the Nth diode is coupled to the ground node.

In re claim 13, Lin discloses the device of claim 9, wherein the transistor functions as a lateral bipolar transistor such that the first junction region comprises an emitter and the second junction region comprises a collector.

In re claim 14, Lin discloses a semiconductor device, comprising:

A substrate (30) having a first conductivity type;

A source region and a drain region in the substrate and separated by a channel region, the source and drain regions having a second conductivity type (N+); and

A gate electrode (12) overlying the channel region and separated therefrom by a gate dielectric layer,

Wherein the channel region extends from the source region to the drain region, and

Wherein a junction between the source region and the channel region functions as an emitter and a junction between the drain region and the channel region functions as a collector,

Whereby an absence of LDD extension regions in the channel region provides relatively low parasitic MOS capacitance between the channel region and the gate electrode.

In re claim 15, Lin discloses the device of claim 14, wherein the source region is coupled to a signal node of an MOS circuit and the drain regions is coupled to a ground node of the MOS circuit. Note that Lin discloses these relationships in the reverse order, but it is well known in that by changing the direction of current flow, the source becomes the drain and vice-versa. Therefore, though the disclosure discloses the source coupled to the ground node and the drain to the signal node, the disclosure still anticipates the claim.

In re claim 16, Lin discloses the device of claim 15, wherein a thickness of the gate dielectric layer substantially the same as the gate dielectric thickness of the MOS circuit (section [0019])

In re claim 17, Lin discloses the device of claim 14, wherein the gate electrode further comprises dielectric sidewall spacers overlying the channel region adjacent to opposing sides of the gate electrode, and wherein the opposing sides of the gate overlie the channel region at a point away from the source and drain regions.

In r e claim 18, Lin discloses the device of claim 14, wherein the MOSFET is configured to support a voltage of greater than about 2.5 volts is across the source and drain regions (section [0040], Table 1).

In re claim 19, Lin discloses the device of claim 14, wherein the gate electrode is electrically coupled to the substrate.

In re claim 20, Lin discloses the device of claim 14, wherein the channel region is defined by a uniformly doped region of the substrate between the source region and the drain region.

***Claim Rejections - 35 USC § 103***

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee et al. (U.S. Patent No. 5,270,565) in view of Iwai et al. (U.S. Patent No. 5,276,346).

In re claim 1, Lee (Fig. 4) discloses a semiconductor device, comprising:

A substrate (34) having a first junction region (n-) separated from a second junction region (n+) by a substrate region;

A MOS gate electrode (47) overlying the substrate region and separated therefrom by a gate oxide layer (49);

Dielectric sidewall spacers adjacent to opposing sides of the MOS gate electrode and overlying the substrate region;

Wherein the substrate region is defined by a uniformly doped region (P-well) of the substrate between the first junction region and second junction region.

Lee does not expressly disclose dielectric sidewalls adjacent opposing sides of the MOS gate electrode. Iwai (Fig. 21g) discloses the use of spacer regions atop source/drain regions. It would have been obvious to one skilled in the art at the time of the invention to use sidewall spacers as disclosed by Iwai in forming the source/drain regions of Lee for the purpose, for example, of using such layers as masking layers to prevent impurities from extending too far under the gate region which would diminish device performance.

### *Allowable Subject Matter*

7. Claims 4 and 11 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

### *Conclusion*

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jesse A. Fenty whose telephone number is 571-272-1729. The examiner can normally be reached on 5/4-9 1st Fri. Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 571-272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jesse A. Fenty
Examiner
Art Unit 2815

Tom Thomas

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